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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/354,302	07/16/99	MORZANO C	M4065.0176/P

EXAMINER	
LUU, A	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/05/01

MM21/0605

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/354,302	Applicant(s) MORZANO, CHRISTOPHER K.	
	Examiner An T. Luu	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 April 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-56 and 82-98* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *38-46 and 48-55* is/are allowed.

6)☐ Claim(s) *1-8,11-20,23-33,36,37,47,56 and 82-98* is/are rejected.

7)☐ Claim(s) *9,10,21,22,34 and 35* is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Introduction

1. Applicant's amendment filed on 4-20-01 has been received and entered in the case. The rejections set forth in the previous Office Action are partially maintained as indicated below.

Claim Rejections - 35 USC § 112

2. Claims 13, 15-16, 25, 37, 47 and 56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 is rejected for being misdescriptive due to the recitation of phrase "in parallel". There is no two transistors of figures 2 and 3 are "in parallel". By definition in electricity, two devices are in parallel, if and only if, their voltage drops are equal. There is no such thing disclosed in figures.

Claim 16 is rejected for the same reason set forth in claim 15.

Phrase "in parallel" is incorrectly used in claims 13, 25, 37, 47 and 56. These claims are rejected for the same reason set forth in claim 15.

Claim Rejections - 35 USC § 102

3. Claims 1-3, 6-8, 14-17, 19-20, 26-33, 36, 82-86 and 91-94 are rejected under 35 U.S.C. 102(e) as being anticipated by the Houston et al. reference (U.S. Patent 6,037,808).

The Houston et al. reference discloses in figure 10 an apparatus comprising a first and a second signal input/output lines (at nodes DOUT and /DOUT) for receiving first and a second

input signals (DOUT and /DOUT) and transmitting first and second outputs signals (DOUT and /DOUT); and a first and second inverters (T13, T4 and T5, T14) connected as a latch (output of each inverter is coupled to input of the other) as recited in claim 1.

As to claim 2, figure 1 discloses an enable circuit (T3 and T15) for receiving an enable signal (/SENSE) for enabling or disabling the first and second inverters in response to the enable signal.

As to claims 3 and 6-7, figure 1 shows a first voltage source (Ground) for supplying a first voltage to the first and second inverter via an N-channel transistor T3 responsive to the enable signal SENSE; a second voltage source (Vdd) for supplying a second voltage to the first and second inverter via an P-channel transistor T15 responsive to the inverse of the enable signal (/SENSE). It is inherent that an inverter is needed to inverting the enable signal to achieve its complementary signal.

As to claim 8, elements T3 and T15 are qualified as first, second input buffers wherein SENSE and /SENSE are qualified as first and second external signals as required by claim.

As to claims 14 and 15, barring the term "in parallel", the recitation of these claims read on figure 1 of the cited reference (i.e., first n- and p-transistors are T4 and T13; second n- and p-transistors are T5 and T14).

As to claim 16, the scope of this claim is similar to the scope of the combination of claims 1, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claim 17, the scope of this claim is similar to the scope of the combination of claims 1, 2, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claim 19, the scope of this claim is similar to the scope of the combination of claims 1, 2, 6, 7, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claim 20, the scope of this claim is similar to the scope of the combination of claims 1, 8, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claims 26-33 and 36, the scopes of these claims are identical to those of claims 1-8 and 12, respectively. Thus, they are rejected for the same reasons set forth above.

As to claims 82-86 and 91-94, they are rejected as being directed to the method or/and steps derived from the apparatus described in claims 1-3 and 6-8 above.

4. Claims 1 and 11are rejected under 35 U.S.C. 102(b) as being anticipated by the Oh reference (U.S. Patent 5,838,173).

The Oh reference discloses in figure 2 an apparatus comprising a latch 27 being configured as required by claim 1 and a first (25) and a second (28) driver circuits connecting to the first (A) and second (B) input/output lines, respectively, for boosting the output signal as required by claim 11.

Claim Rejections - 35 USC § 103

5. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Houston et al. reference (U.S. Patent 6,037,808).

The Houston reference discloses all the limitation required by claims 4-5 except for showing a proper type of transistors (i.e., n- and p-type transistors) connected to the first and

second voltage sources. It is notoriously well known in the art that N- and P-type transistors are complementary transistors and they can be used interchangeably. Thus, it would have been obvious for one skilled in the art to use either type of transistor in his circuit since the selection between complementary transistors is seen as design expedient dependent upon the particular of the application.

6. Claims 12-13 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Oh reference (U.S. Patent 5,838,173) in view of the Garcia reference (U.S. Patent 5,949,259).

The Oh reference discloses all the claimed limitations recited in claims 12 and 13 including a driver circuit. The Oh reference does not disclose a specific structure of the driver circuit as recited in claims. The Garcia reference discloses in figure 6 a driver circuit comprising at least a first and a second driver inverter (202; P4 and N4) connected in series; and a third inverter (P2,N3) wherein the third inverter and the series connected inverters have the same input and the output of the third inverter connected to a device N1 such that the output of the series connected inverters is set to a predetermined voltage as understood by claim 13 based on figure 5 of the instant application. It would have been obvious for one skilled in the art to replace a generic driver circuit taught by Oh with the one taught by Garcia because the skilled artisans will easily recognize that a driver circuit can be implemented in many different ways in the art, one of such way is as shown in the Garcia for controlling a slew-rate of an output buffer circuit.

The scopes of claims 36-37 are similar to those of claims 12-13. Therefore, they are rejected for the similar reason set forth above.

7. Claims 18, 23-25, 87-90 and 95-98 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Houston et al. reference (U.S. Patent 6,037,808) as applied to claims 1-3, 6-8 and 14-15 above, in view of the Oh reference (U.S. Patent 5,838,173) and further in view of the Garcia reference (U.S. Patent 5,949,259).

As to claim 18, the scope of this claim is similar to the scope of the combination of claims 1, 2, 3, 4, 5, 14 and 15. Thus, it is rejected for the same reasons set forth above.

As to claim 23, the scope of this claim is similar to the scope of the combination of claims 1, 11, 14, 15 and 16. Thus, it is rejected for the same reasons set for above.

As to claim 24, the scope of this claim is similar to the scope of the combination of claims 1, 11, 12, 14, 15 and 16. Thus, it is rejected for the same reasons set for above.

As to claim 25, the scope of this claim is similar to the scope of the combination of claims 1, 11, 12, 13, 14, 15 and 16. Thus, it is rejected for the same reasons set for above.

As to claim 87-90 and 95-98, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Response to Arguments

8. Applicant's arguments filed 4-20-01 have been fully considered but they are not persuasive.

As to the rejections under 102 with respect to the Houston reference for claims 1-3, 6-8, 14-17, 19-20, 26-33, 36, 82-86 and 91-94, Applicant has argued that the operation of his

invention is different from that of the prior art. Examiner respectfully disagrees because the rejections were based on the recitation of claims, not what disclosed in the body of specification. Further, Applicant has argued that T13 and T4 transistors (likewise transistors T5 and T14) do not form an inverter; and DOUT and /DOUT are merely output lines, not input/output lines. Again, Examiner respectfully disagrees because each pair of transistors T13 - T4 and T5-T14 are configured as inverter as known in the art. DOUT and/DOUT lines are input/output lines because transistors T13 - T4 and T5-T14 are forming a latch circuit as shown in figure 10. Thus, the output of one inverter is an input of the other, and vice versa.

As to the rejections under 102 with respect to the Oh reference for claims 1 and 11, Applicant has argued that "the latch in figure 2 of Oh has one input line B and one output line C. The latch 27 in Oh does not have a first and second input/output lines" as required by claim. Examiner respectfully disagrees because line B is also seen as output line due to feedback via device 29 and inverter (22,23), so is line C.

As to the rejections under 103 with respect to the Houston reference for claims 4-5, Applicant's argument is the same as presented previously (i.e., T13 - T4 and T5-T14 are not inverters). The same reason set forth above is applicable here.

As to the rejections under 103 with respect to the Oh reference in view of Garcia for claims 12 and 13, Applicant has argued that there is no motivation to combine these references. Examiner respectfully disagrees because Oh does have input/output lines and a driver circuit can be implemented in many different ways as known in the art. One of such ways is shown by Garcia.

Allowable Subject Matter

9. Claims 38-46 and 48-55 are allowed.

10. Claims 9-10, 21-22 and 34-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 47 and 56 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to discloses an apparatus comprising elements being configured as recited in claims. Particularly, none of the prior art discloses a differential amplifier and a circuit for reducing skewing as claimed.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication should be directed to An T. Luu whose phone number is (703)-308-4922 and facsimile number is (703)-308-7722.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reach on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to group receptionist at (703)-308-0956.

An T. Luu

May 27-01

TIMOTHY P CALLAHAN
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